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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,027	09/30/2003	Dennis Kim	RAMB-01016US0	5412

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DENIRO/RAMBUS
575 MARKET STREET
SUITE 2500
SAN FRANCISCO, CA 94105

EXAMINER	
PANWALKAR, VINEETA S	
ART UNIT	**PAPER NUMBER**
2611	

MAIL DATE	DELIVERY MODE
02/05/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/675,027	KIM ET AL.	
	Examiner	Art Unit	
	Vineeta S. Panwalkar	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-8,10-30,32 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,5-8 and 10-24* is/are allowed.

6)☒ Claim(s) *25-30 and 33* is/are rejected.

7)☒ Claim(s) *32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/10/08 has been entered.

Claim Objections

2. Claim30 is objected to because of the following informalities: It is suggested that in line 6, "an adjust signal" should be replaced by – the adjust signal--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 25, 28-30 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 6041090), hereinafter, Chen in view of Nakamura (US 20020030522 A1), hereinafter, Nakamura.

3a. Regarding claims 25 and 33, Chen discloses a phase locked loop (PLL) (Fig. 8) system (claimed circuit of claim 25 and corresponding means as per claim 33) comprising:

- a sampler (Fig. 8, data sampler 26) configured to output a plurality of digital data signals (Fig. 8, digital data signals (D1 –D5)) in response to a clock signal (Fig. 8, clock signal 24) (Also see Fig.2 , column 3, lines 43-63 and column 5, lines 47-65);
- a phase detector (Fig. 8, phase detectors 34, 94 and 104 are together interpreted as claimed phase detector) to output a plurality of up

signals (Fig. 8, UP signals 35A, 98A and 108A) and a plurality of down signals (Fig. 8, DOWN signals 35B, 98B and 108B) in response to the plurality of digital data signals (Also see Fig.2 , column 3, lines 43-63 and column 5, lines 47-65);

- a clock circuit (Fig. 8, charge pumps 36, 96 and 106, loop filter 38 and clock generator 22 are together interpreted as claimed clock circuit) configured to generate the clock signal in response to phase adjust signals (Fig. 8, signals UP and DOWN signals are interpreted as phase adjustment signals) (Column 3, lines 43-63).

Thus, Chen shows all the limitations claimed, but fails to explicitly show whether the clock circuit whether the phase adjustment signal may be output by an averaging circuit.

However, in the same field of endeavor, Nakamura shows a clock generator wherein

- the clock circuit comprises, an averaging circuit (Fig. 5, unit 15 performs claimed averaging; see paragraph [0076]) capable to output the phase adjust signal (Fig. 8, output of unit 15 is interpreted as claimed phase adjust signal) in response to an average up signal, obtained from a plurality of up signals in a predetermined period of time, and an average down signal, obtained from a plurality of down signals, in the predetermined period of time (Paragraphs [0072]-[0077]).

Thus, it would have been obvious to a person of ordinary skill in the art to use the averaging circuit shown by Nakamura in the Chen's circuit because Nakamura's averaging circuit serves as a filter for blocking high-frequency components (Paragraph [0076])and hence prevents jitter characteristics from being lowered to generate high-quality clocks (Paragraph [0024]).

3b. Regarding claim 28, Chen and Nakamura disclose all the limitations claimed.

Chen further shows that the circuit is included in a receive circuit coupled to a transmit circuit capable of transmitting the data signal.(Column 1, lines 27-30, wherein the recovery circuit is interpreted as being in claimed receive circuit and transmit and receive circuit are interpreted as being coupled via fiber-optic cables).

3c. Regarding claim 29, Chen discloses a phase locked loop (PLL) (Fig. 8) system (claimed apparatus) comprising:

- a transmit circuit capable of transmitting a data signal .(Column 1, lines 27-30); and
- a receive circuit capable of generating a clock signal in response to the data signal (Column 1, lines 27-30);
- wherein the receive circuit includes:

- a sampler (Fig. 8, data sampler 26) outputting a plurality of digital data signals (Fig. 8, digital data signals (D1 –D5)) in response to the clock signal (Fig. 8, clock signal 24) and the data signal (Fig. 8, data signal 21) (Also see Fig.2 , column 3, lines 43-63 and column 5, lines 47-65);
- a phase detector (Fig. 8, phase detectors 34, 94 and 104 are together interpreted as claimed phase detector) to output a plurality of up signals (Fig. 8, UP signals 35A, 98A and 108A) and a plurality of down signals (Fig. 8, DOWN signals 35B, 98B and 108B) in response to the plurality of digital data signals (Also see Fig.2 , column 3, lines 43-63 and column 5, lines 47-65);
- a clock circuit (Fig. 8, charge pumps 36, 96 and 106, loop filter 38 and clock generator 22 are together interpreted as claimed clock circuit), coupled to the sampler, capable of generating the clock signal in response to phase adjust signals (Fig. 8, signals UP and DOWN signals are interpreted as phase adjustment signals) (Column 3, lines 43-63).

Thus, Chen shows all the limitations claimed, but fails to explicitly show whether the clock circuit whether the phase adjustment signal may be output by an averaging circuit.

However, in the same field of endeavor, Nakamura shows a clock generator wherein the clock circuit comprises:

- an averaging circuit (Fig. 5, unit 15 performs claimed averaging; see paragraph [0076]) capable of outputting the phase adjust signal (Fig. 8,

output of unit 15 is interpreted as claimed phase adjust signal) in response to an average up signal, obtained from the plurality of up signals in a predetermined period of time, and an average down signal, obtained from the plurality of down signals, in the predetermined period of time (Paragraphs [0072]-[0077]).

Thus, it would have been obvious to a person of ordinary skill in the art to use the averaging circuit shown by Nakamura in the Chen's circuit because Nakamura's averaging circuit serves as a filter for blocking high-frequency components (Paragraph [0076])and hence prevents jitter characteristics from being lowered to generate high-quality clocks (Paragraph [0024]).

3d. Regarding claim 30, Chen discloses a timing recovery phase locked loop (PLL) wherein is disclosed a method for tracking a comprising the steps of:

- receiving the signal (Column 1, lines 27-30).;
- outputting a plurality of digital data signals in response to an adjust signal (Fig.8, adjust signals 37, 97, 107) and the signal (Fig. 8, data signal 21) (Also see Fig.2 , column 3, lines 43-63 and column 5, lines 47-65, wherein sampler 26 outputs plurality of digital data signals D1-D5 in response to clock based on adjust signals 37, 97 and 107 and data signal 21)

- selecting an update rate (Column 5, line 42 – column 6, line 3, wherein strobing the incoming data at a different rate is interpreted as selecting an update rate); and
- selecting the adjust signal in response to the signal (See Figs.2 and 8, column 3, lines 43-63 and column 5, lines 47-65), wherein adjust signals 37, 97 and 107 are interpreted as adjust signals).

Thus, Chen discloses all the limitations claimed (including plurality of up signals (Fig. 8, UP signals 35A, 98A and 108A) and a plurality of down signals (Fig. 8, DOWN signals 35B, 98B and 108B)), but fails to explicitly disclose claimed averaging and adjustable step-size.

In the same field of endeavor, however, Nakamura discloses a PLL system wherein is disclosed a method including:

- averaging a plurality of up signals to obtain an average up value; averaging a plurality of down signals to obtain an average down value; outputting the adjust signal in response to the average up value and average down value. (Fig. 5, unit 15 performs claimed averaging; see paragraph [0076]) and output of unit 15 is interpreted as claimed phase adjust signal with adjustable step-size. The step size is interpreted as being adjustable because it is an average of several up and down signals and hence changes each time it is averaged).

Thus, it would have been obvious to a person of ordinary skill in the art to use the averaging circuit shown by Nakamura in the Chen's circuit because Nakamura's averaging circuit serves as a filter for blocking high-

frequency components (Paragraph [0076])and hence prevents jitter characteristics from being lowered to generate high-quality clocks (Paragraph [0024]).

4. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Nakamura as applied to claim 25 above, and further in view of Shastri (US 2002/0105386 A1, previously cited), hereinafter, Shastri.

4a. Regarding claim 26, Chen and Nakamura disclose all the limitations claimed (see 2a above).

However, Chen and Nakamura fail to explicitly disclose claimed counter.

In the same field endeavor however, Shastri discloses a clock recovery circuit, wherein is disclosed a counter capable of outputting phase adjust signal. (Figs 12,13 and 14. Counter 41 takes in UP4 and DOWN4 signals. The output of the counter 41 is fed to a comparator 43 (paragraphs [0067]-[[0068]) and then is further used to output a phase adjust signal (paragraph [0094]). Thus, counter 41 is required to generate the phase adjustment and is hence interpreted as claimed mixer counter).

Thus, it would have been obvious to a person of ordinary skill in the art to use the circuit suggested by Shastri because it prevents glitches in the generated clock. (Paragraph [0012]).

4b. Regarding claim 27, Chen and Nakamura disclose all the limitations claimed (see 2a above).

However, Chen and Nakamura fail to explicitly disclose claimed comparison.

In the same field endeavor however, Shastri discloses a clock recovery circuit, wherein:

- the averaging circuit includes a comparator circuit, capable of adjusting the phase adjust signal in response to a comparison of the average up value and the average down value. (Figs 12,13 and 14. Counter 40 keeps a running average of the up and down indications of the phase detector and outputs UP4 and DOWN4. Slow filter 47 keeps track of the average of the UP4/DOWN4 signals thereby maintaining a running average of the total UP/DOWN indication count. A rollover and resulting PHUP or PHDOWN signifies that there is a strong indication that the RCK has drifted permanently away from the phase of the input data DIN, i.e. indicating phase adjust. (See paragraph [0091],[0092]). Thus, counter 41 takes in UP4 and DOWN4 signals and the output of the counter 41 is fed to a comparator 43 (paragraphs [0067]- [[0068]) and then is further used to output a phase adjust signal (paragraph [0094])).

Thus, it would have been obvious to a person of ordinary skill in the art to use the circuit suggested by Shastri because it prevents glitches in the generated clock. (Paragraph [0012]).

Allowable Subject Matter

5. Claim 32 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

5a. Regarding claim 32, prior art of record fails to show a method for tracking signals wherein selecting an adjustable step-size includes determining a first step-size based on a variable data bit-rate of the signal; determining a second step-size and summing the first and second step sizes to obtain adjustable the step-size, in combination with each and every other limitation of the base claim.

6. Claims 1-3, 5-8, 10-24 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

6a. Regarding claim 1, prior art of record fails to show a circuit comprising a clock generating circuit capable of generating a clock signal in response to and adjustable phase step-size and sampler with a data signal having a variable rate and including at least four stages wherein the clock circuit includes stall logic for capable of holding the third and fourth stage outputs in response to the first and second stage outputs, in combination with

every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs 1 and 5.

6b. Claims 2, 3, 5-8, 12 and 13 are allowed as being dependent on claim 1.

6c. Regarding claim 10, prior art of record fails to show the circuit comprising capable of generating a clock signal in response to and adjustable phase step-size and sampler with a data signal having a variable rate, wherein the clock circuit includes a counter for obtaining a first step-size and the indicator provides a second step-size, wherein the first step size and the second step size are summed to obtain the adjustable phase step-size, in combination with every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs. 1 and 7.

6d. Claim 11 is allowed as being dependent on claim 10.

6e. Regarding claim 14, prior art of record fails to show a circuit with a clock circuit comprising a first stage, coupled to the sampler, capable of outputting a first stage output signal in response to the data signal; a second stage, coupled to the first stage, capable a second stage output signal in response to the first of outputting stage output signal', a third stage, coupled to the second stage, capable outputting the phase adjust signal in response to the second stage output signal; and stall logic, coupled to the first, second and third stages, and capable of holding the phase adjust signal in response to the first and second stage output

signals, in combination with every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs 1 and 5.

6f. Claims 15-17 will be allowable as being dependent on claim 14.

6g. Regarding claim 18, prior art of record fails to show a circuit with a clock circuit comprising a first stage, coupled to the sampler, capable of outputting a first stage output signal in response to the data signal; a second stage, coupled to the first stage, capable of outputting a second stage output signal in response to the first stage output signal; a third stage, coupled to the second stage, capable of outputting the phase adjust signal, having a first step-size, in response to the second stage output signal; stall logic, coupled to the first, second and third stages, capable of holding the phase adjust signal in response to the first and second stage output signals; an indicator, coupled to the third stage, capable of outputting a second step-size in response to the variable data bit- rate; and, a counter, coupled to the third stage and the indicator, capable of outputting the phase adjust signal having an adjustable step-size responsive to the first and second step-sizes, in combination with every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs 1, 5 and 7.

6h. Claims 19-24 are allowed as being dependent on claim 18.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays,

should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vineeta S. Panwalkar whose telephone number is 571-272-8561. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VP

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER